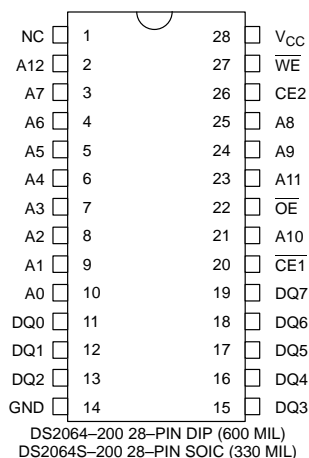


## FEATURES

- Low power CMOS design
- Standby current
  - 50 nA max at  $t_A = 25^\circ\text{C}$   $V_{CC} = 3.0\text{V}$
  - 100 nA max at  $t_A = 25^\circ\text{C}$   $V_{CC} = 5.5\text{V}$
  - 1  $\mu\text{A}$  max at  $t_A = 60^\circ\text{C}$   $V_{CC} = 5.5\text{V}$
- Full operation for  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$
- Data Retention Voltage =  $5.5\text{V}$  to  $2.0\text{V}$
- Access time equals 200 ns at  $5.0\text{V}$
- Operating temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- Full static operation
- TTL compatible inputs and outputs
- Available in 28-pin DIP and 28-pin SOIC packages
- Suitable for both battery operated and battery backup applications

## PIN ASSIGNMENT



## PIN DESCRIPTION

A0–A12	– Address Inputs
DQ0–DQ7	– Data Input/Output
$\overline{\text{CE1}}$ , CE2	– Chip Enable Inputs
$\overline{\text{WE}}$	– Write Enable Input
$\overline{\text{OE}}$	– Output Enable Input
$V_{CC}$	– 5V Power Supply Input
GND	– Ground
NC	– No Connection

## DESCRIPTION

The DS2064 is a 65536-bit low power, fully static random access memory organized as 8192 words by eight bits using CMOS technology. The device operates from a single power supply with a voltage input between 4.5V and 5.5V. The chip enable inputs ( $\overline{\text{CE1}}$  and CE2) are used for device selection and can be used in order to achieve the minimum standby current mode, which fa-

cilitates both battery operate and battery backup applications. The device provides fast access time of 200 ns and is most suitable for low power applications where battery operation or battery backup for nonvolatility are required. The DS2064 is a JEDEC-standard 8K x 8 SRAM and is pin-compatible with ROM and EPROM of similar density.

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING
$V_{CC}$	Power Supply Voltage	-0.3V to +7.0V
$V_{IN}, V_{I/O}$	Input, Input/Output Voltage	-0.3 to $V_{CC} + 0.3V$
$T_{STG}$	Storage Temperature	-55°C to +125°C
$T_{OPR}$	Operating Temperature	-40°C to +85°C
$T_{SOLDER}$	Soldering Temperature/Time	260°C for 10 seconds

**RECOMMENDED DC OPERATING CONDITIONS** $(t_A = -40^{\circ}C \text{ to } +85^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	
Input High Voltage	$V_{IH}$	2.0		$V_{CC} + 0.3$	V	
Input Low Voltage	$V_{IL}$	-0.3		0.8	V	
Data Retention Voltage	$V_{DR}$	2.0		5.5	V	

**DC CHARACTERISTICS** $(t_A = -40^{\circ}C \text{ to } +85^{\circ}C; V_{CC}=5V \pm 10\%)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	$I_{IL}$	$0V \leq V_{IN} \leq V_{CC}$			$\pm 0.1$	$\mu A$
I/O Leakage Current	$I_{LO}$	$\overline{CE1}=V_{IH}, 0V \leq V_{IO} \leq V_{CC}$			$\pm 0.5$	$\mu A$
Output High Current	$I_{OH}$	$V_{OH} = 2.4V$	-1.0			mA
Output Low Current	$I_{OL}$	$V_{OL} = 0.4V$	4.0			mA
Standby Current	$I_{CCS1}$	$\overline{CE1} = 2.0V$			0.5	mA
Standby Current	$I_{CCS2}$	$\overline{CE1} \geq V_{CC} - 0.5V, t_A = 60^{\circ}C$			1	$\mu A$
Standby Current	$I_{CCS2}$	$\overline{CE1} \geq V_{CC} - 0.5V, t_A = 25^{\circ}C$			100	nA
Operating Current	$I_{CCO}$	$\overline{CE1} = 0.8V, 200 \text{ ns cycle}$			70	mA

**CAPACITANCE** $(t_A = 25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

# AC CHARACTERISTICS, READ CYCLE

( $t_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC}=5\text{V} \pm 10\%$ )

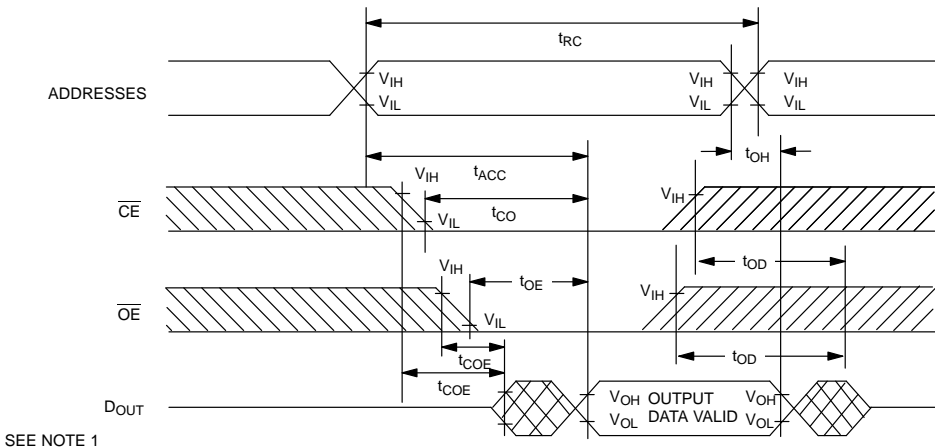
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	$t_{RC}$	200			ns	
Access Time	$t_{ACC}$			200	ns	
$\overline{OE}$ to Output Valid	$t_{OE}$			100	ns	
$\overline{CE}$ to Output Valid	$t_{CO}$			200	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	$t_{COE}$	5			ns	
Output to High-Z from Deselection	$t_{OD}$	10		60	ns	
Output Hold from Address Change	$t_{OH}$	5			ns	

# AC CHARACTERISTICS, WRITE CYCLE

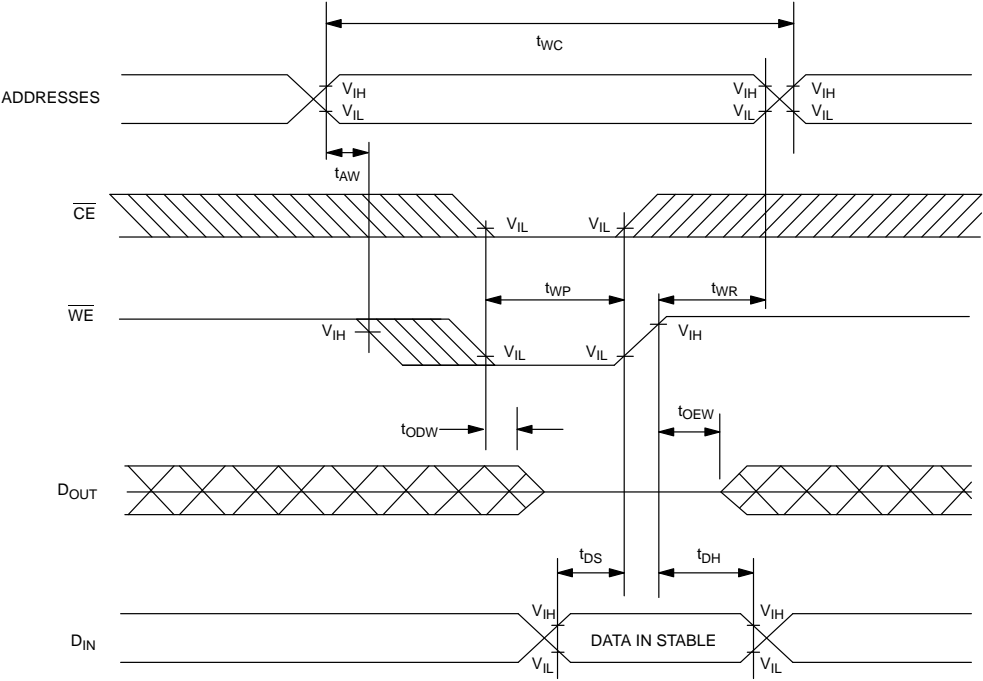
( $t_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC}=5\text{V} \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	$t_{WC}$	200			ns	
Write Pulse Width	$t_{WP}$	150			ns	
Address Setup Time	$t_{AW}$	0			ns	
Write Recovery Time	$t_{WR}$	10			ns	
Output High-Z from $\overline{WE}$	$t_{ODW}$			70	ns	7
Output Active from $\overline{WE}$	$t_{OEWE}$	5			ns	7
Data Setup Time	$t_{DS}$	80			ns	
Data Hold Time	$t_{DH}$	0			ns	

# TIMING DIAGRAM: READ CYCLE

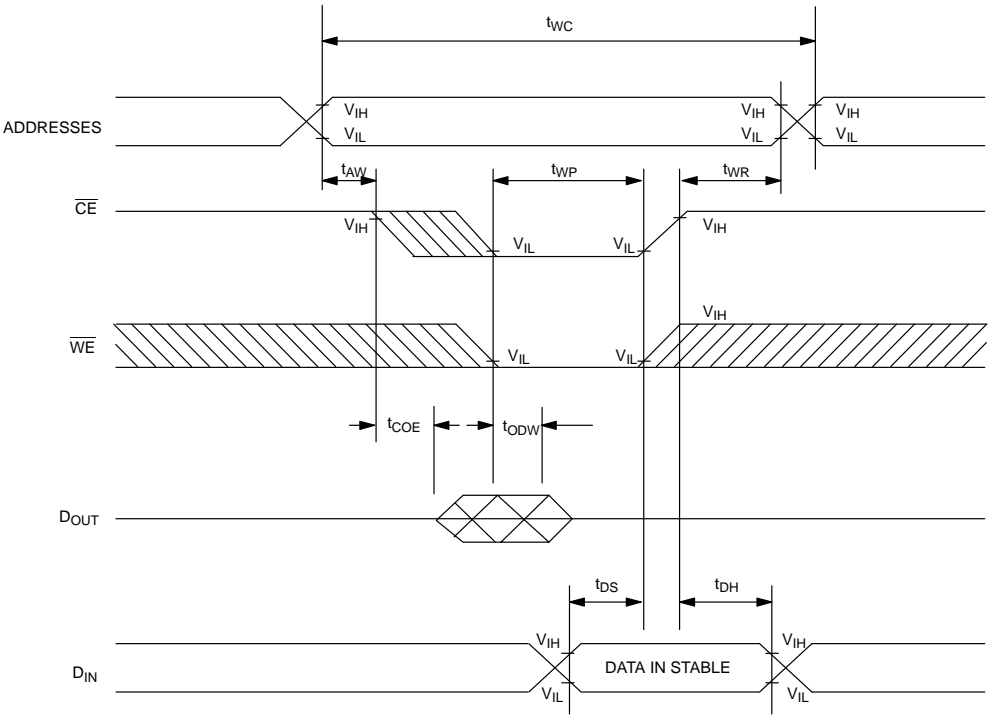


TIMING DIAGRAM: WRITE CYCLE 1



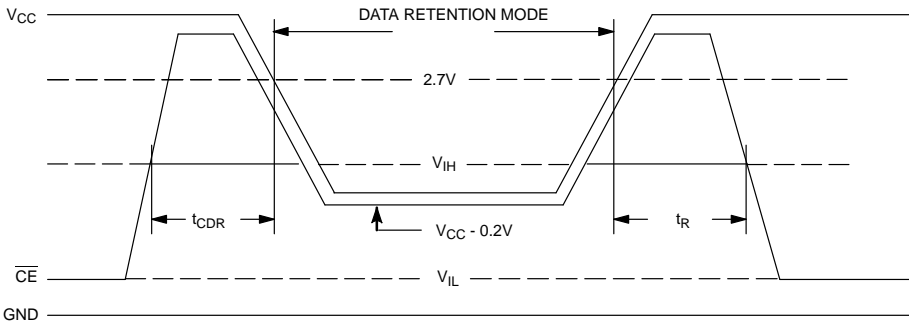
SEE NOTES 2, 3, 4, 5, 6 AND 7

# TIMING DIAGRAM: WRITE CYCLE 2



SEE NOTES 2, 3, 4, 5, 6 AND 7

# TIMING DIAGRAM: DATA RETENTION – POWER UP, POWER DOWN



SEE NOTE 8

DATA RETENTION CHARACTERISTICS

(t<sub>A</sub>=−40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Supply Voltage	V <sub>DR</sub>	$\overline{\text{CE1}} \geq V_{\text{CC}} - 0.5\text{V}$	2.0		5.5	V
Data Retention Current at 5.5V	I <sub>CCR1</sub>	$\overline{\text{CE1}} \geq V_{\text{CC}} - 5.0\text{V}$		0.1*	1	μA
Data Retention Current at 2.0V	I <sub>CCR2</sub>	$\overline{\text{CE1}} \geq V_{\text{CC}} - 5.0\text{V}$		50*	750	nA
Chip Deselect to Data Retention	t <sub>CDR</sub>		0			μs
Recovery Time	t <sub>R</sub>		2			ms

\* Typical values are at 25°C

FUNCTION TABLE

MODE	$\overline{\text{CE1}}$	CE2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0 – A12	DQ – DQ7	POWER
READ	L	H	L	H	STABLE	DATA OUT	I <sub>CCO</sub>
WRITE	L	H	X	L	STABLE	DATA IN	I <sub>CCO</sub>
DESELECT	L	H	H	H	X	HIGH-Z	I <sub>CCO</sub>
STANDBY	H	X	X	X	X	HIGH-Z	I <sub>CCS</sub>
STANDBY	X	L	X	X	X	HIGH-Z	I <sub>CCS</sub>

**NOTES:**

1.  $\overline{WE}$  is high for read cycles.
2.  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
3.  $t_{WP}$  is specified as the logical AND of  $\overline{CE}$  and  $\overline{WE}$ .  $t_{WP}$  is measured from the latter of  $\overline{CE}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
4.  $t_{DH}$  and  $t_{DS}$  are measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
5. If the  $\overline{CE}$  low transition occurs simultaneously with or latter than the  $\overline{WE}$  low transition, the output buffers remain in a high impedance state.
6. If the  $\overline{CE}$  high transition occurs prior to or simultaneously with the  $\overline{WE}$  high transition, the output buffers remain in a high impedance state.
7. If  $\overline{WE}$  is low or the  $\overline{WE}$  low transition occurs prior to or simultaneously with the  $\overline{CE}$  low transition, the output buffers remain in a high impedance state.
8. If the  $V_{IH}$  level of  $\overline{CE}$  is 2.0V during the period that  $V_{CC}$  voltage is going down from 4.5V to 2.7V,  $I_{CCS1}$  current flows.

**DC TEST CONDITIONS**

Outputs Open

All voltages are referenced to ground

**AC TEST CONDITIONS**

Output Load: 100 pF + 1TTL Gate

Input Pulse Levels: 0V – 3.0V

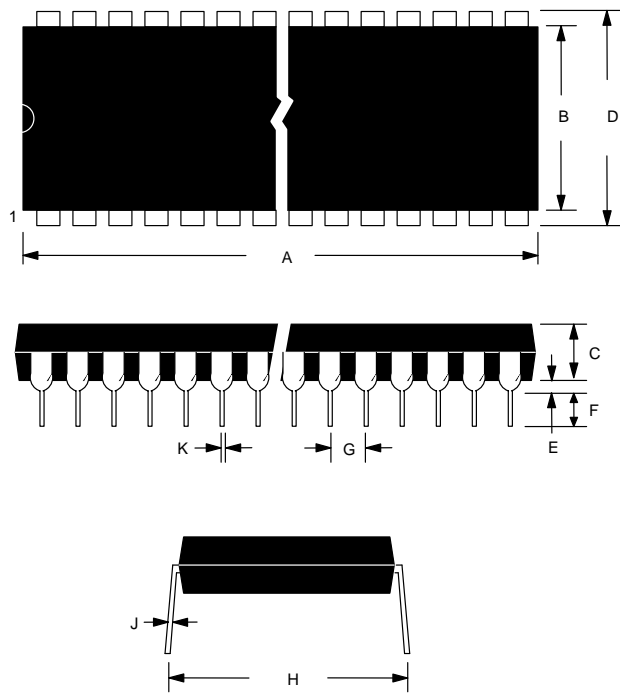
Timing Measurement Reference Levels

Input: 1.5V

Output: 1.5V

Input Pulse Rise and Fall Times: 5 ns

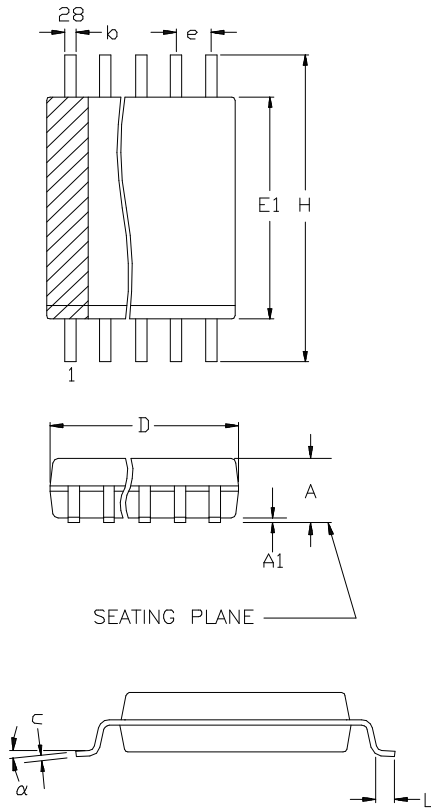
DS2064 28-PIN DIP



PKG	28-PIN	
	DIM	
	MIN	MAX
A IN.	1.440	1.460
MM	30.99	32.00
B IN.	0.540	0.560
MM	13.72	14.22
C IN.	0.140	0.160
MM	3.56	4.06
D IN.	0.590	0.625
MM	14.99	15.88
E IN.	0.015	0.040
MM	0.380	1.02
F IN.	0.110	0.135
MM	2.79	3.43
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.625	0.675
MM	15.88	17.15
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



# DS2064S 28-PIN SOIC



PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	0.080 2.04	0.120 3.05
A1 IN. MM	0.002 0.05	0.014 0.35
b IN. MM	0.012 0.30	0.020 0.50
C IN MM	0.004 0.10	0.0125 0.32
D IN. MM	0.697 17.70	0.728 18.50
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN. MM	0.324 8.23	0.350 8.90
H IN MM	0.453 11.5	0.500 12.7
L IN MM	0.016 0.40	0.051 1.30
$\alpha$	0°	10°

The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.